GAS Journal of Engineering and Technology (GASJET)

Volume 2, Issue 8, 2025 Journal Homepage: https://gaspublishers.com/gasjet-home/ ISSN: 3048-5800
Email: editor@gaspublishers.com

Residual Stress in Multilayer NTC Thermistors during Bending Test

RyongJin O[1], TaeYong Yun[2], HyonGyu Pak[3], NamChol Yu[1*]

[1]Kim Chaek University of Technology, Pyongyang, Democratic People's Republic of Korea
[2]PyongSong University of Education, Pyongsong, Democratic People's Republic of Korea
[3]Sariwon University of Education, Sariwon, Democratic People's Republic of Korea

Received: 19.08.2025 | **Accepted:** 09.09.2025 | **Published:** 24.09.2025

***Corresponding Author:** NamChol Yu

DOI: 10.5281/zenodo.17186628

Abstract **Original Research Article**

The stress occurred on the NTC (negative temperature coefficient) thermistor chip while serving process of the chip was investigated in this study. We built 3D models of NTCs and examined the stresses in chip inside with varying structures, on varying load conditions; structural bending load, temperature cycling load, separately and both. In the resistor ceramic body around termination regions which were connected with solders, the stresses had relatively significant values than the other regions and it was considered as a main factor of the failure of NTC body. When the number of the inner-electrodes increased, the maximum principle stress occurred on the inside of NTC was decreased gradually and when the number of electrodes was equal to 24, it had the lowest value as 524 MPa. Also, the stress changes of inside on varying times were investigated when the periodic temperature of the chip body was changed from -60 ℃ to 120 ℃. In this case, the maximum principle stress had the lowest value as 538 MPa also when the number of inner-electrode was also equal to 24. In addition, stress distribution patterns of bending load were compared with temperature cycling load. Through this study optimized geometry and failure condition of NTC were obtained.

Keywords: Residual Stress, Multilayer, NTC Thermistors, Bending Test.

1. Introduction

The NTC thermistor chips have been used widely in electronics applications such as automatics and aerospace and etc.

These have been adopted effectively as temperature sensing unit, temperature compensation unit of reference voltage source for its specific characteristic which the resistance of that is related directly to temperature. Many researches on the NTC have developed up to date and from the requirement of miniaturization and high-speed of electronic devices, it has demanded to improve the reliability and operation characteristic of that.

In most temperature sensing applications, the NTC thermistors are made of spinel manganite [1, 2]. Thick film thermistors based on complex spinel $(Mn, Co, Fe, Cu)_3O_4$ powder with binding glass have been known for more than two decades now [3, 4]. Nanometric thermistor paste was developed in the last decade using the complex spinel mentioned above [5, 6], then characterized and applied for printing of different types of thermistors [7]. The thick film thermistor has several types such as sandwich, multilayer, segmented and interdigitated and the calculating methods of resistivity and B value by these types were described in [8]. In Miura et.al [9], it was reported that the flexural strength was the maximum when the amount of Ni substitution was x = 0.25, and decreased rapidly when x exceeded 0.25 for $(Mn_{1-x}Ni_x)_3O_4$ volume NTC thermistor ceramics and was primarily concerned with the residual stresses induced by the cooling process that follows sintering.

The NTC consists of several inner electrodes which are enclosed by thermistor ceramic material and three-layer terminations which are connected to ceramic body.

Metallic oxide materials such as NiO, Mn_3O_4, Co_3O_4, Cu_2O_3, Fe_2O are used as a thermistor material, and these materials form complex spinel $(Mn, Co, Fe, Cu)_3O_4$ structure. [3, 10].

To improve the characteristics and reliability of electronic chip, many researches have been focused on getting optimized structure and finding proper material of the chips. One part of the researches was implemented to test chips by using experimental apparatuses and the other part was implemented by simulation programs.

With the advent of highly efficient computers and reliable simulation programs, in most case, by testing methods based on simulation programs, we used to test characteristics of chip and studied to get optimized conditions for operation.

The stresses in multilayer thermistors can be simulated through the finite element method (FEM), calculated by analytical models, measured by X-ray diffraction (XRD) [9]. Compared with other techniques, the FEM provides a convenient approach to analyze detailed local stress information within multilayer structures [11-14]. Many test results showed that the test method based on experiment was similar nearly to the method based on simulation method [15, 16]. Thus by using the simulation tools, we can not only support the reliable result, but also enhance the reliable application spaces of the chip by apply special conditions (high pressure, high humidity, complex boundary conditions) which are difficult to apply in experimental method.

The stress distributions of the chip on thermal load and mechanical bending load take an importance place in simulation of stress which are occurred in NTC, and the other effects are subordinated to above conditions.

Also, now the effects of NTC by unknown factors such as pressure, humidity around of chip are obscure. Many factors influence to characteristics of the chip, the structures and material properties are main factors [17]. Also, structure and material of solder which is used to mount the chip onto board (PCB) which are affected to characteristic of the chip [18].

The thermal stress occurs in sintering, soldering [19] and operating processes and the mechanical stress occurs by the bending load of pressure after mounted onto PCB (printed circuit board).

Under these processes and conditions, from the differences of material properties such as thermal expansion coefficient, modulus of elasticity of NTC elements, the stresses are focused on the boundary sides and if it lasts for a long time, the NTC tends to be failure.

The deformation behavior of the thermistor and the board is assumed to be elastic, and the plastic deformation of the metals is described by a bilinear kinematic hardening law [20].

There were many advances to improve operating characteristics of NTCs, however effect of complex load condition of structural bending and thermal loads was not discussed apparently in any study.

In this study, we fundamentally considered the stress distribution and principle stress of ceramic body, electrodes, boundaries of inner electrodes, soldered region, three-layered terminations, then simulated and analyzed for optimization of NTC design.

It is obvious that if the dimension of NTC structure is enhanced, bending resistance will be improved. However, from the requirement of miniaturization of NTC, the aspect geometrical dimensions are maintained and researches tend to change only inner structures. In this study, we didn't discuss the effect of termination structures and solder profile. The stresses which were occurred in NTC on temperature-cycling/bending load conditions were analyzed completely.

If the inner structure of NTC is changed, the stresses of noted region will be changed.

Then by considering of stress distribution which is occurred inside of NTC, the dangerous region will be predicted and the failure will be prevented.

From the study on the effect of number of inner electrodes to MPS (maximum principle stress), the optimized number was obtained.

The NTC models in simulation were built as 3-D model and these models are more realistic and necessary to consider the effect of several factors in complex structure.

All the simulations of the study were implemented with FEM by using ANSYS 19.0 simulation program and we analyzed the results concretely.

2. Modeling and Method

Modeling

In this study, we discussed 3-D model which consists thermistor ceramic body, electrodes surrounded by the ceramic and terminations of 3-layers as the Fig 1 shows.

Here, thermistor ceramic body is the material of (Mn, Ni, $Fe)_2O_3$ prepared according to the sol-gel auto combustion.

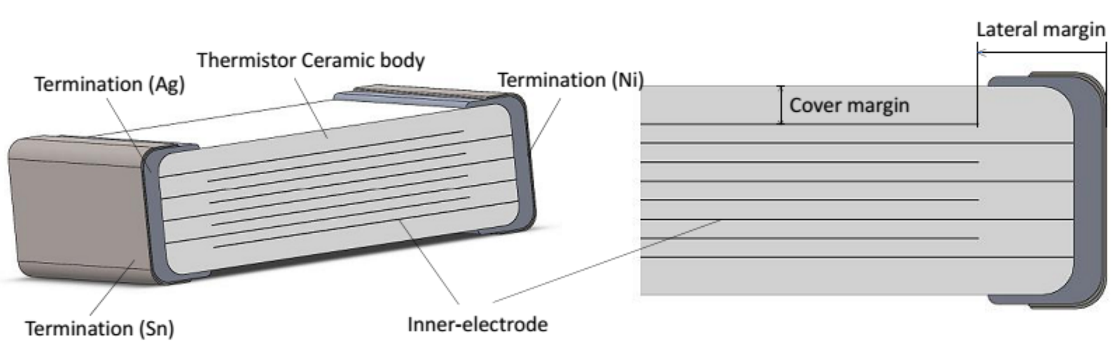


Fig 1. Schematic structure of multi-layer NTC thermistor; thermistor ceramic body, inner-electrodes and 3-layer termination

The dimensions of the selected multilayer NTC thermistor are 1850 × 1150 × 550 ㎛ (2012 type) same as NTCG204CH104J ($R_{25\ °C}$ = 100 kΩ, $B_{25/85\ °C}$ = 4150 K ± 3 %, TDK Corporation, Japan).

The model in fig.1 has 8 inner electrodes which has 2 ㎛ thickness. The thickness of electrodes and dimension between electrodes of all the models in the simulation are maintained as 2 ㎛ and 14 ㎛. The cover layer may be changed according to number of electrodes. The material of electrodes is selected as *Ag* and electrodes are arranged alternatively and cumulated. Inner electrodes are arranged apart from both side ends with a dimension of 300 ㎛ and connected with terminations electrically, mechanically.

The section side of termination of 3-layer consists materials of *Ag*, *Ni* and *Sn*, also the thicknesses of the section are 75 ㎛, 6 ㎛, 6 ㎛ in transversal direction and 25 ㎛, 6 ㎛, 6 ㎛ in longitudinal direction separately.

In the model, the lateral margin, housing margin and cover margin are 300 ㎛, 300 ㎛, 100 ㎛ separately.

The following table 1, 2, 3 show the properties of materials used in this simulation.

The NTC was mounted onto copper pad of PCB with solder.

To build models like this, we designed the solder model like a triangular as shown the Fig 2 and the solder supports the connection of the termination and copper pad of PCB.

More details, solder profile was shaped as triangular while connecting under side of NTC terminations with copper pad of PCB.

The material of solder is led- free and it was reported that the led-free solder shows a benefit in comparison to softer tin-lead [17]. The dimensions of PCB were determined as 300×70×1.15mm and the NTC was placed on the center of the PCB.

The model of NTC connected with PCB and meshed element are shown in Fig 2.

Table 1. Properties of the metal materials at various temperatures (silver, nickel, tin and copper)

Materials	Properties	Values						
		-50 ℃	-25 ℃	0 ℃	25 ℃	100 ℃	200 ℃	300 ℃
Silver (inner electrode)	Elastic modulus (GPa)	73	72.2	71.8	71.2	71	70.5	69
	Poisson’s ratio	0.37	0.37	0.37	0.37	0.37	0.37	0.37
	Yield stress (MPa)	29	28.5	28	27.5	26.3	11	8.5
	Thermal expansion coefficient(10^{-6}/K)	17.5	18	18.5	19.21	19.27	29.33	19.41
Nickel (middle terminal layer)	Elastic modulus (GPa)	213	211	209	207	205	203	200
	Poisson’s ratio	0.31	0.31	0.31	0.31	0.31	0.31	0.31
	Yield stress (MPa)	63	62	61	60	59	57	56
	Thermal expansion coefficient(10^{-6}/K)	13	13.1	13.2	13.3	13.5	13.8	14.1
Tin (final terminal layer)	Elastic modulus (GPa)	47	46	45	44.3	40,4	38.5	38.5
	Poisson’s ratio	0.33	0.33	0.33	0.33	0.33	0.33	0.33
	Yield stress (MPa)	20	18	16	14.5	11	4.5	4.5
	Thermal expansion coefficient(10^{-6}/K)	17	19	22	23	25	28.9	28.9
Copper (PCB)	Elastic modulus (GPa)	130	127	125	123	120	117	90
	Poisson’s ratio	0.31	0.31	0.31	0.31	0.31	0.31	0.31
	Yield stress (MPa)	43	42	41	40	38	32	31
	Thermal expansion coefficient(10^{-6}/K)	16	16.1	16.3	16.5	16.8	18.2	18.4

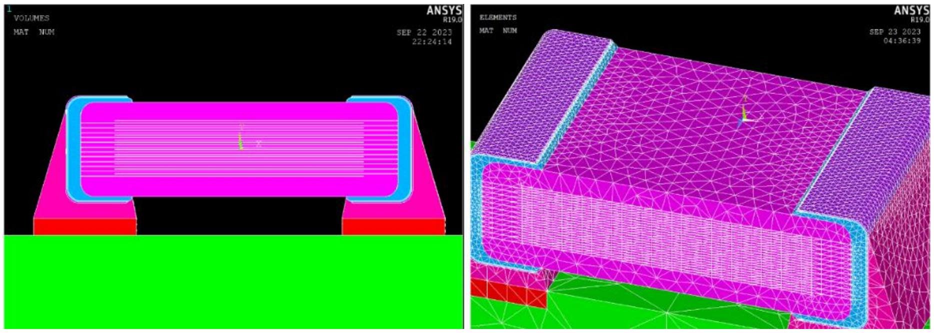


Fig 2. NTC model (Left) soldered on PCB and meshed element (Right)

Table 2. Properties of the (Mn, Ni, Fe)$_3$O$_4$-based thermistor ceramic and cover glass at various temperatures

Materials	Properties	Value						
		-50 ℃	-25 ℃	0 ℃	25 ℃	100 ℃	200 ℃	300 ℃
(Mn, Ni, Fe)$_3$O$_4$ - based thermistor ceramic	Elastic modulus (GPa)	176	178	180	182	198	204	204
	Poisson’s ratio	0.33	0.33	0.33	0.33	0.33	0.33	0.33
	Thermal expansion coefficient ($\times 10^{-6}$/K)	7.6	7.8	8	8.2	8.6	9.4	10.4
Cover glass	Elastic modulus(GPa)	142	143	144	145	146	149	150
	Poisson’s ratio	0.33	0.33	0.33	0.33	0.33	0.33	0.33
	Thermal expansion coefficient($\times 10^{-6}$/K)	13	13	13.1	13.2	14.1	16.2	17.2

Table 3. Properties of solder (20Sn-80Pb)

Properties	Value			
	-60 ℃	0 ℃	25 ℃	100 ℃
Elastic modulus (GPa)	39	36.5	32.5	22.9
Poisson’s ratio	0.36	0.36	0.36	0.36
Yield stress (MPa)	40	36.4	15.2	5.8
Thermal expansion coefficient (10^{-6}/K)	24.7	24.7	24.7	24.7

Method

FEM (finite element method) is a numerical method which divides model into finite count of element, then solves boundary problems in all boundaries with approximation functions by considering initial conditions, and induces the total result.

To improve accuracy of simulation result, fine meshing is required, the important thing is to determine meshing resolution according to structure and dimensions of model reasonably. In other word, it has not worth to determine the meshing resolution of chip same as the PCB. The elements which have small dimensions and have to be considered carefully ask fine meshing resolution. Following this, not only high simulation speed but also high accuracy can be presented. The simulations in this study brought high precision of result by fine meshing of electrodes and terminations.

The objects which have symmetric structure like NTCs can be simulated and resulted as half model, but in this study, we used model of total NTC connected with PCB because the model got bending loads.

And the element shape is important in improved accuracy. There are two elements shape - rectangle and triangular then here triangular shape is selected because the model has complex shape and rounded surfaces.

We can define element type as a SOILD185 in mechanical analysis and SOLID 278 in thermal analysis. Also mechanical degrees of the model for bending stress can be contained to SOLID 278 as a structural load in thermal analysis.

The model was meshed as 387412 elements totally and 282421 elements of NTC body. Thus the NTC body takes place 72 % of total element approximately.

The simulation has the following two steps.

1. Mechanical bending step with constant volume temperature of 25 ℃.
2. Step of 2-cycling volume temperature with above condition.

The four points of PCB were selected and two points of both ends were fixed in all DOF, either two points were displaced 1mm perpendicularly to PCB to apply mechanical bending load.

The following Fig 3 shows the principles of 4-point bending [21].
But for structural bending load of thermistor in simulation the both end-side of the PCB were displaced in all DOFs (degree of freedom).
For the simulation of temperature cycling, the thermal load was applied to the chip for 30 minutes by temperature changing from -60 ℃ to 120 ℃ in two times.
The fig.4 shows the temperature cycling condition used in the second step simulation.

The assumptions used in simulations are like;
1. NTC was in stress free at the initial situation (beginning situation of simulation)
2. Perfect bonding exists between different materials, such as the thermistor ceramic and the termination layers of the NTC, and the solder material and the PCB.
3. The thermal residual stress results from the different coefficients of thermal expansion of the materials employed.
4. Convection and radiation were not taken into account during total processes.

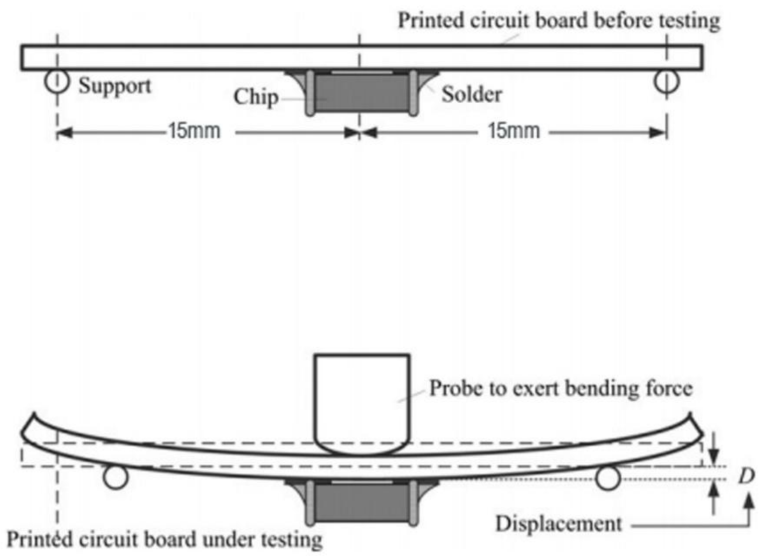


Fig 3. Schematic drawing of mechanical bending load

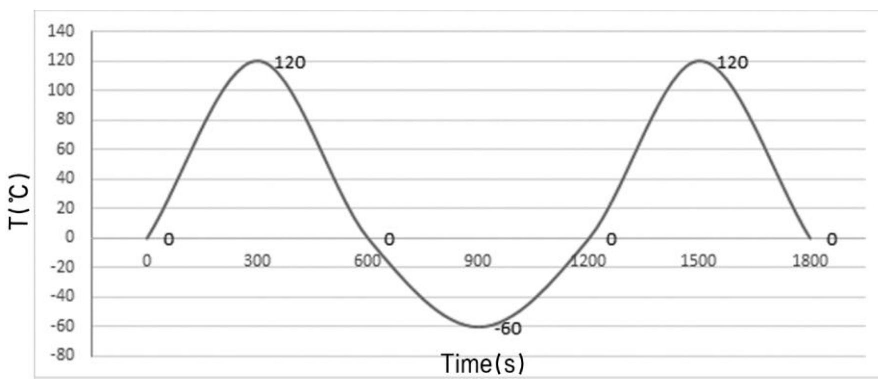


Fig 4. Temperature changes of NTC body according to times.

3. Result and Discussion

The stresses which were occurred in NTC inside when exert bending load were simulated.
The Fig 5 (Left) shows the stresses of NTC inside in bending test with condition of temperature.

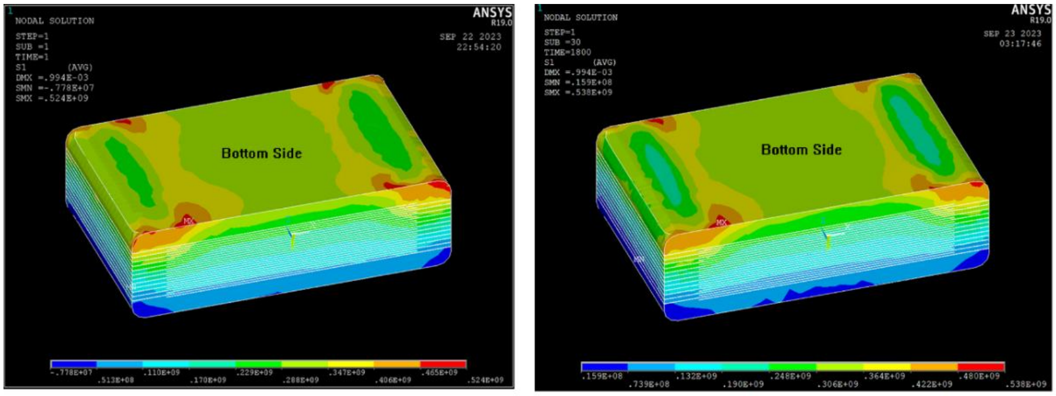
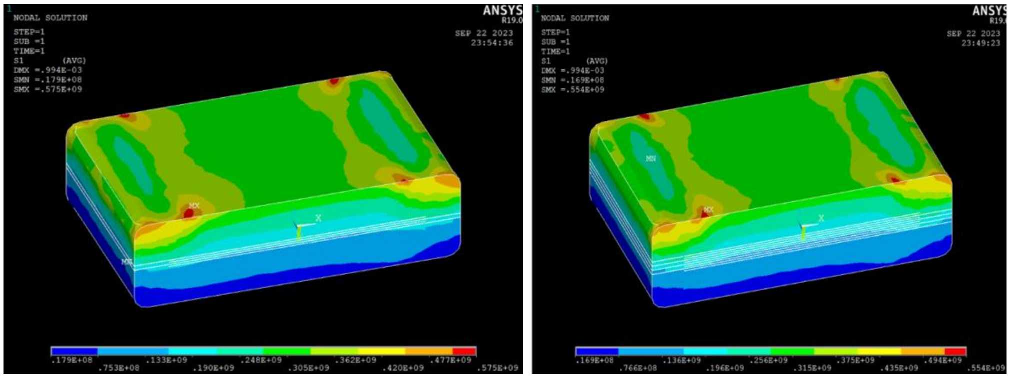


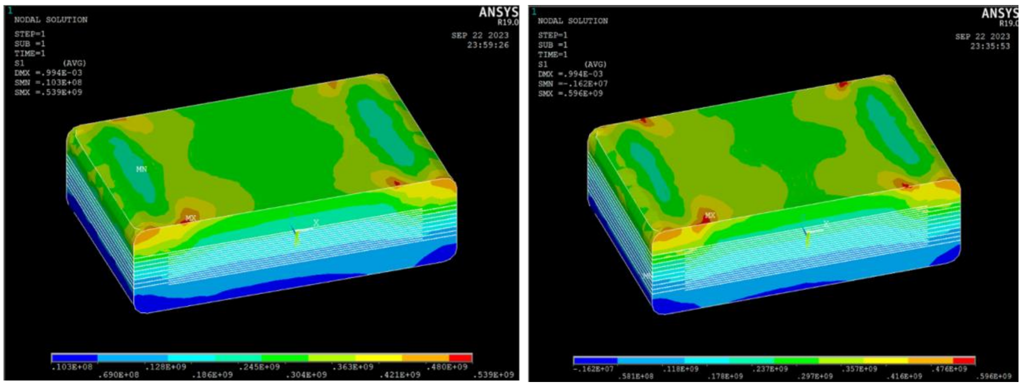
Fig 5. Stress distribution pattern on bending load (Left) and bending+temperature cycling load (Right)

The model was built by 24-electrodes, thickness of electrode as 2 ㎛, division distance of electrode as 14 ㎛, and other dimensions were according to the noted value above.
The bottom line of Fig 5 indicates the stress values according to colors.
From the result Fig 5 (Left), in the bending load state, the red partition's stress was maximum value as 524 MPa and the blue was minimum value as -7.78 MPa.
The positive value means compressed state, the negative value means tensile state.
By the reason of bending of PCB, the top side of NTC used to take tension stress and bottom side used to take compression stress. The stresses are focused on red point of bottom side of terminations which are contacted with solder, these stresses are used to originate the failure. While bending of PCB, the chip was stressed in PCB-copper pad-solder-NTC surface ordering, and the stress was concentrated on the red point because the bottom side of chip was surrounded by solder. Also, the stresses were observed on the same bending condition while changing the temperature of NTC volume from -60 ℃ to 120 ℃ during 2-cycles. In this case, as the Fig 5 (Right) shown, difference stresses were occurred compared with the only bending condition.
The maximum stress (SMX) was 538 MPa and minimum stress (SMN) was -15.9 MPa, which were recorded as different value (524 MPa, -7.78 MPa) on bending condition. Also, stress distribution of top, bottom and profile sides of NTC are different compared with bending load condition. Considering the right pattern of Fig 5 corresponds to last state of bending + temperature cycling load with temperature of 0 ℃, it is appeared that the residual thermal stress affect to total stresses. It seems that if the state lasts for a long time, the chip may have failure because of high fatigue.
Compared with bending load state, in bending + temperature cycling load state SMX showed miner increasing but SMN showed about 2-times increasing.
Also, more considerable stress distribution was appeared in top side of NTC.

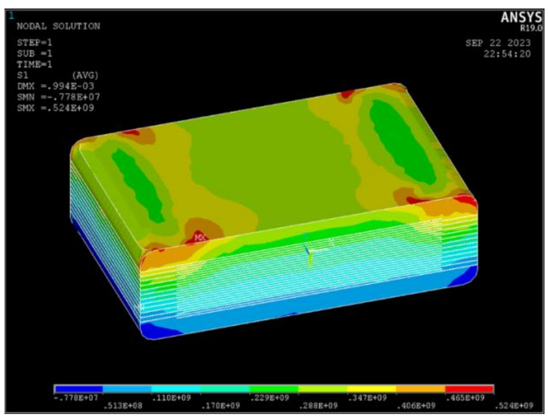
Maximum stresses according to number of electrodes of NTC were obtained while changing the electrode number from 4 to 24.
The results of bending and temperature cycling tests are explained in following Fig 6, Fig 7. According to the Fig 6 and Fig 7, the stress distribution of bending + temperature cycling test propagated from local section of inside to surface and more considerable stress was exerted to electrode side. This phenomenon is due to additional thermal stress in NTC body.
Following curves (Fig 8, 9) show the minimum and maximum stress versus number of electrodes. By increasing the number of electrodes, noted stresses were decreased and it was expected that the stress may have saturation curve by increasing the number. So the more number of inner-electrodes, the lower stress in ceramic body. However from the requirement of chip manufacturing and miniaturization, the number of inner-electrode will be limited to 24.
More important thing is that by increasing number of inner-electrodes, stress distribution slop can be reduced, this may be connected to improvement of NTC performance. Compared with bending test, in the case stress on top side of NTC had different value. In bending test, stress change was vague on the top side, but considerable tensile stress was occurred in termination connection sides. This behavior has the reason of CTE (thermal expansion coefficient) differences between terminals and thermistor ceramic materials. While changing temperature from negative to positive value, tensile stress occurred to top side on NTC because the solder, Sn, Ni, Ag and thermistor ceramic materials had different CTEs, also this stress are imposed on the tensile force of board bending.
Fig 10 shows SMX/SMN values occurred in NTC during total simulation. Red and Blue lines indicate SMX and SMN separately. As the Fig 10 shown, the curves has symmetric shape by centering on time of 900s, the temperature of that time is minimum value as -60 ℃. At the moment, SMN has a relatively big absolute value, also the region of the SMN is intended inside not on surface. The region of SMN at the moment is also considered as critical factor of failure.



(a) 4-electrodes (b) 8-electrodes

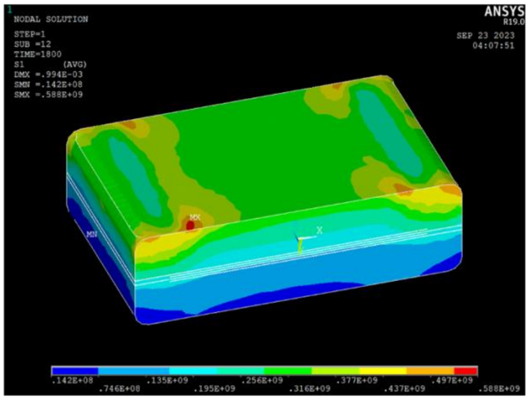
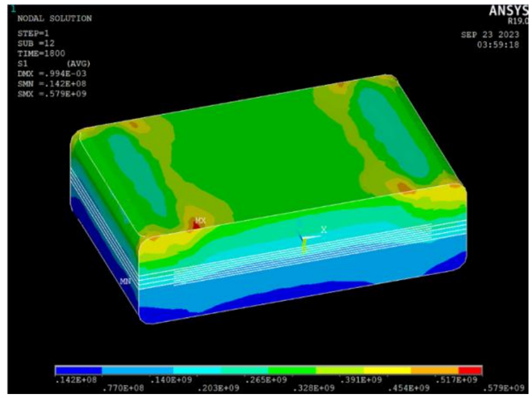


(c) 16-electrodes (d) 20-electrodes

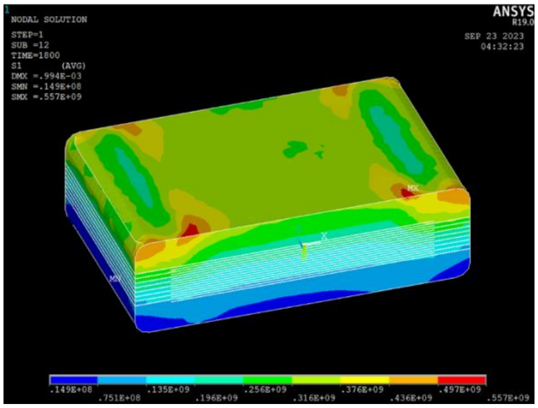
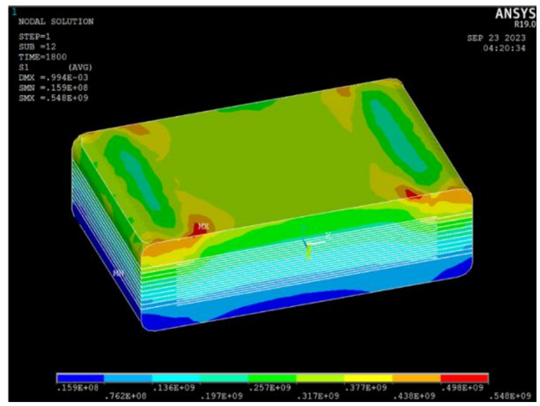


(e) 24-electrodes

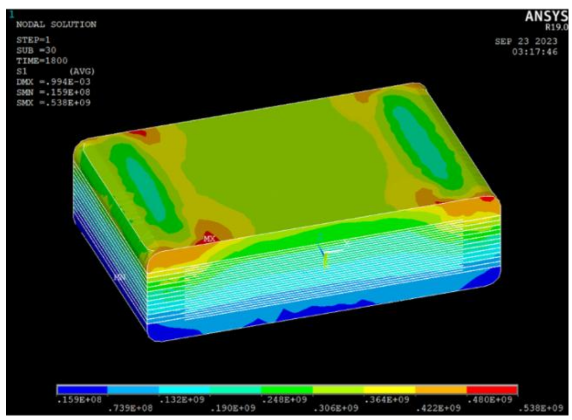
Fig 6. Stress distribution pattern on bending load with varying inner-electrodes :(a) 4-electrodes (b) 8-electrodes (c) 16-electrodes (d) 20-electrodes (e) 24-electrodes

(a) 4-electrodes (b) 8-electrodes

(c) 16-electrodes (d) 20-electrodes



(e) 24-electrodes

Fig 7. Stress distribution pattern on bending + temperature cycling load with varying inner-electrodes; (a) 4-electrodes (b) 8-electrodes (c) 16-electrodes (d) 20-electrodes (e) 24-electrodes

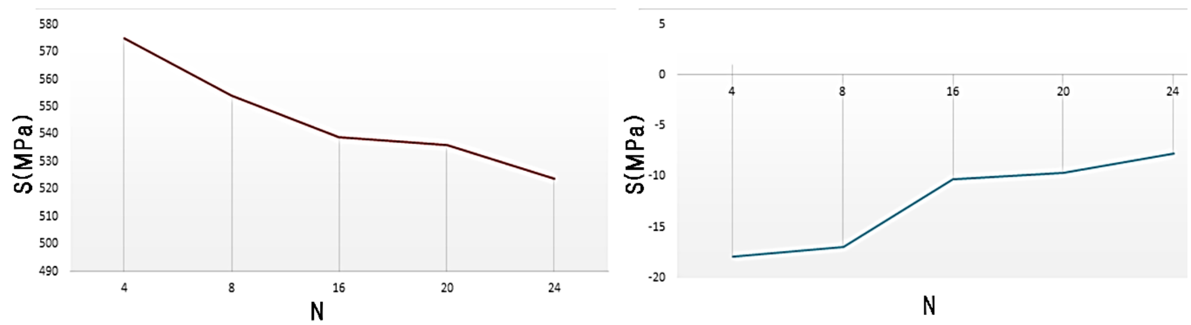


Fig 8. Maximum (Red line) and minimum (Blue line) stress changes within varying number of inner-electrodes on bending load. Horizontal and vertical axis correspond to number of inner-electrode and stress separately.

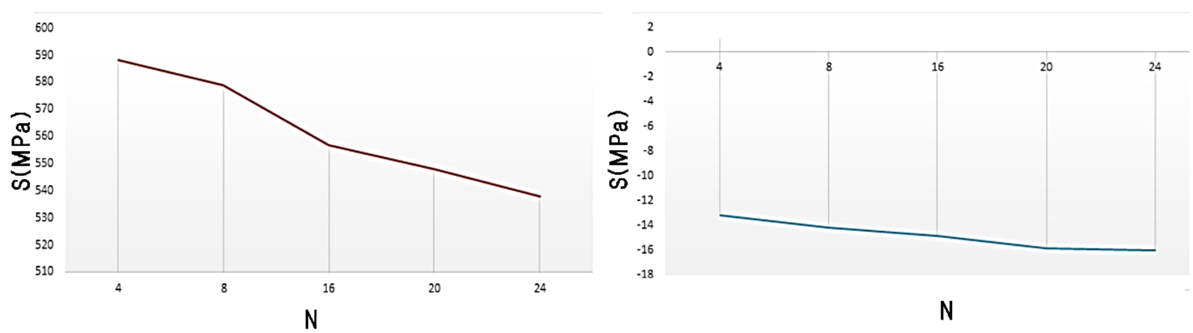


Fig 9. Maximum (Red line) and minimum (Blue line) stress changes within varying number of inner-electrodes on bending + temperature cycling load at the final time of simulation. Horizontal and vertical axis correspond to number of inner-electrode and stress separately.

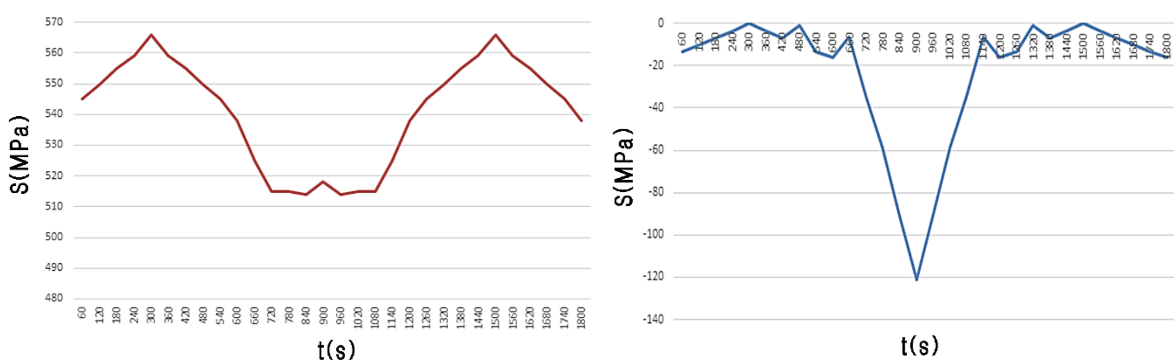


Fig 10. Maximum (Red line) and minimum (Blue line) stress changes according to times on bending + temperature cycling load. Horizontal and vertical axis correspond to simulation time and stress separately.

4. Conclusion

The study on stress occurred in NTC body subordinated in PCB were presented. The three-dimensional model closed to real NTC was built and the result was obtained by FEM in load condition of four-point bending. The result of simulation shows that when increase number of electrodes of NTC, stress distribution in NTC body will be changed and this affects to the lifetime of NTC. Furthermore, to reveal the operation characteristics of NTC in more realized atmosphere, stress occurred in NTC body was observed by FEM within combination load condition of bending and temperature-cycling.

According to the result of simulation, stress distribution of the combination load condition is certainly different with only bending condition, then the values of maximum and minimum stress were different comparatively and the SMX and SMN had the lowest absolute value at the time of 900s. Also, SMX and SMN had the lowest values when number of inner-electrodes was 24, the behavior revealed the optimized number of electrodes.

By using these simulation methods worked in this study, the more concreted and realized investigation on operation characteristics of devices such as MLCC (multilayer ceramic capacitor) and chip resistor will be implemented. Future work will investigate operation characteristics of devices with more realized conditions (temperature, humidity, convection, electro-caloric effect and etc).

References

[1] Maclen E. D. (1979) Thermistors. Glasgow, Electrochemical Publications, pp 12–67

[2] Vakiv M. (2001) Controlled thermistor effect in the system CuxNi1-x-yCo2yMn2-yO4. J Eur Ceram Soc 21:1783–1785. https:// doi.org/10.1016/s0955-2219(01)00115-7

[3] Altenburg H. (2001) Semiconductor ceramics for NTC thermistors: the reliability aspects. J Eur Ceram Soc 21:1787–1791. https://doi.org/10.1016/s0955-2219(01)00116-9

[4] Fritsch S. (1998) Correlation between the structure, the microstructure and the electrical properties of nickel manganite negative temperature coefficient (NTC) thermistors. Solid State Ion 109:229–237. https://doi.org/10.1016/S0167-2738(98)00080-0

[5] Aleksic´ O. S. (2017) Recent advances in NTC thick film thermistor properties and applications. Electron Energ 30:267–284. https:// doi.org/10.2298/fuee1703267a

[6] Ikegami A. (1980) Thick-film thermistor and its applications. IEEE Trans CHMT 3:541–550. https://doi.org/10.1109/TCHMT.1980. 1135644

[7] Yadav BC (2019) Temperature sensors based on semiconducting oxides: an overview. http://arxiv.org/pdf

[8] Aleksic´ OS (2007) Modeling and simulation of NTC thick film thermistor geometries. Microelectron Int 24:27–34

[9] Miura T. (2007) Material design for high strength NTC thermistor ceramics. Electroceram Jpn X 350:229–232. https://doi.org/10. 4028/www.scientific.net/KEM.350.229

[10] Buchanan R. C. (2019) Ceramic materials for electronics, third edition, revised and expanded. CRC Press. ISBN 9780367394134

[11] Ali R., Sebastiani M. (2015) Influence of Ti-TiN multilayer PVDcoatings design on residual stresses and adhesion. Mater Des 75:47–56. https://doi.org/10.1016/j.matdes.2015.03.007

[12] Guo-Liang Yu (2015) Theoretical investigation of magnetoelectric effect in multilayer magnetoelectric composites. Compos Struct 119:738–748. https://doi.org/10.1016/j.compstruct.2014.09.049

[13] Li Q. (2016) Fabrication of SiNx thin film of micro dielectric barrier discharge reactor for maskless nanoscale etching. Micromachines 7:232–241. https://doi.org/10.3390/mi7120232

[14] Treml R. (2016) High resolution determination of local residual stress gradients in single-and multilayer thin film systems. Acta Mater 103:616–623. https://doi.org/10.1016/j.actamat.2015.10.044

[15] Smith N. A. S. (2014) Experimentally validated finite element model of electrocaloric multilayer ceramic structures. Journal of Applied Physics 116, 044511 (2014); https:// doi.org/10.1063/1.4891298

[16] Chang-Wei Huang (2015) Finite Element Analysis and Design of Thermal-Mechanical Stresses in Multilayer Ceramic Capacitors. Int. J. Appl. Ceram. Technol., 12 [2] 451–460 (2015). https:// doi.org /10.1111/ijac.12176

[17] Gilad Sharon (2011) Modeling Stress Responses of Multilayer Capacitors Using Varying Termination Geometries, J Fail. Anal. and Preven. (2011) 11:546–551. https:// doi.org10.1007/s11668-011-9480-x

[18] Ciprian Rizescu (2010) Simulation and Experimental Validation of Bond Strength of a Surface Mount Chip Capacitor. Mechatronics 2010, June 28 - 30, Swiss Federal Institute of Technology ETH, Zurich Switzerland

[19] Nam Chol Yu (2020) The effects on residual stress in multilayer NTC thermistors during soldering process and bending test (I. soldering process). Microsystem Technologies (2020) 26:3765–3771. https://doi.org/10.1007/s00542-020-04855-0

[20] Davis J. R. (1998) Metals handbook, desk edition. ASM International, Cleveland. ISBN 978-0-87170-654-6

[21] International standard IEC 6060539-1:2016 and IEC 6060 539-2:2019